

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Case outline X change dimension D and dimension L max. Update boilerplate.	97-07-03	R. MONNIN
B	Case outline "X" dimensions L, R, and R1 are updated. -rrp	97-12-02	R. MONNIN
C	Replaced reference to MIL-STD-973 with reference to MIL-PRF-38535. Replaced figure 1 with reference to standard figure in MIL-STD-1835. - gt	03-09-03	R. MONNIN
D	Update boilerplate paragraphs. - ro	09-09-08	C. SAFFLE
E	Update drawing to current MIL-PRF-38535 requirements. Removed class M references. -rrp	16-07-19	C. SAFFLE

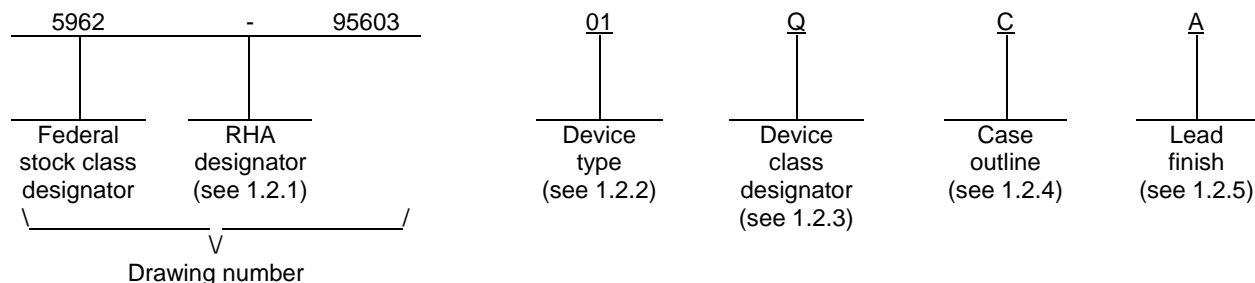


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REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E					
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11								
PMIC N/A	PREPARED BY RAJESH PITHADIA				DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil															
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY RAJESH PITHADIA																			
	APPROVED BY MICHAEL A. FRYE				MICROCIRCUIT, LINEAR, CMOS, PRECISION, DUAL/QUAD, MICROPOWER, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON															
	DRAWING APPROVAL DATE 96-04-25																			
	REVISION LEVEL E				SIZE A	CAGE CODE 67268		5962-95603												
					SHEET 1 OF 11															

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LMC6462A	Precision CMOS dual micropower operational amplifier
02	LMC6464A	Precision CMOS quad micropower operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line
X	GDFP1-G14	14	Flat pack with gullwing leads

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

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1.3 Absolute maximum ratings. 1/

Supply voltage (V+ - V-)	16 V
Differential input voltage	±Supply voltage
Voltage at input/output pin	(V+) + 0.3 V, (V-) – 0.3 V
Current at input pin	±5 mA <u>2/</u>
Current at output pin	±30 mA <u>3/ 4/</u>
Current at power supply pin	40 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (PD):	
Device type 01	3 mW
Device type 02	6 mW
Lead temperature (soldering, 10 seconds)	+260°C
Junction temperature (T _J)	+150°C <u>3/</u>
Thermal resistance, junction-to-case (θ _{JC}): <u>5/</u>	
Case outlines C and X	8°C/W
Case outline P	14°C/W
Thermal resistance, junction-to-ambient (θ _{JA}): <u>5/</u>	
Case outline C	74°C/W still air 37°C/W 500 LFPM
Case outline P	122°C/W still air 67°C/W 500 LFPM
Case outline X	132°C/W still air 78°C/W 500 LFPM

1.4 Recommended operating conditions.

Supply voltage	+3.0 V to +15.5 V
Ambient operating temperature range (T _A)	-55°C to +125°C

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
- 3/ Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability. Both single-supply and split-supply operation are affected.
- 4/ Must not connect output to V+ when V+ is greater than 13 V or reliability will be adversely affected.
- 5/ Thermal resistance limits apply for packages soldered directly into a printed circuit board.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1</u> / -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
3 Volt parameters							
Input offset voltage	VOS		1	All		0.8	mV
			2,3			1.7	
Input bias current	IBIAS	<u>2</u> /	1	All		25	pA
			2,3			100	
Input offset current	IOS	<u>2</u> /	1	All		25	pA
			2,3			100	
Common mode rejection ratio	CMRR	0 V ≤ VCM ≤ 3.0 V	1	All	60		dB
			2,3		57		
Input common-mode voltage range	VCM	CMRR ≥ 50 dB	1	All	3.0	0.0	V
			2,3		2.9	0.1	
Supply current	ICC	VO = V+/2	1	01		55	μA
			2,3			70	
			1	02		110	
			2,3			140	
Output short circuit current	ISC	Sourcing, VO = 0 V	1	All	8		mA
			2,3		6		
		Sinking, VO = 3 V	1	All	23		
			2,3		17		
Output voltage swing	VOP	RL = 25 kΩ to V+/2	1	All	2.9	0.10	V
			2,3		2.8	0.15	
5 Volt parameters							
Input offset voltage	VOS		1	All		0.5	mV
			2,3			1.4	
Input bias current	IBIAS	<u>2</u> /	1	All		25	pA
			2,3			100	
Input offset current	IOS	<u>2</u> /	1	All		25	pA
			2,3			100	
Common mode rejection ratio	CMRR	0 V ≤ VCM ≤ 5.0 V	1	All	70		dB
			2,3		67		
Input common-mode voltage range	VCM	CMRR ≥ 50 dB	1	All	5.25	-0.10	V
			2,3		5.00	0.00	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1</u> / -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
5 Volt parameters – continued.							
Supply current	ICC	VO = V+/2	1	01		55	μA
			2,3		70		
			1	02		110	
			2,3		140		
Output short circuit current	ISC	Sourcing, VO = 0 V	1	All	19		mA
			2,3		15		
		Sinking, VO = 5 V	1		22		
			2,3		17		
Output voltage swing	VOP	RL = 100 kΩ to V+/2	1	All	4.990	0.010	V
			2,3		4.980	0.020	
		RL = 25 kΩ to V+/2	1		4.975	0.020	
			2,3		4.965	0.035	
15 Volt parameters							
Input offset voltage	VOS		1	All		1.8	mV
			2,3			2.3	
Input bias current	IBIAS	<u>2</u> /	1	All		25	pA
			2,3			100	
Input offset current	IOS	<u>2</u> /	1	All		25	pA
			2,3			100	
Common mode rejection ratio	CMRR	0 V ≤ VCM ≤ 15.0 V	1	All	70		dB
			2,3		67		
Input common-mode voltage range	VCM	CMRR ≥ 50 dB	1	All	15.25	-0.15	V
			2,3		15.00	0.00	
Positive power supply rejection ratio	+PSRR	5 V ≤ V+ ≤ 15.0 V, V- = 0 V, VO = 2.5 V	1	All	70		dB
			2,3		67		
Negative power supply rejection ratio	-PSRR	-5 V ≤ V- ≤ -15.0 V, V+ = 0 V, VO = -2.5 V	1	All	70		dB
			2,3		67		
Output voltage swing	VOP	RL = 100 kΩ to V+/2	1	All	14.975	0.025	V
			2,3		14.965	0.035	
		RL = 25 kΩ to V+/2	1		14.900	0.050	
			2,3		14.850	0.150	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
15 Volt parameters – continued.							
Supply current	I _{CC}	V _O = V ₊ /2	1	01		60	μA
			2,3			70	
			1	02		120	
			2,3			140	
Output short circuit current	I _{SC}	Sourcing, V _O = 0 V	1	All	24		mA
			2,3		17		
		Sinking, V _O = 12 V <u>3/</u>	1	All	55		
			2,3		45		
Large signal voltage gain	A _V	Sourcing, R _L = 100 kΩ <u>4/</u>	1	All	110		dB
			2,3		80		
		Sinking, R _L = 100 kΩ <u>4/</u>	1		100		
			2,3		70		
		Sourcing, R _L = 25 kΩ <u>4/</u>	1		110		
			2,3		70		
		Sinking, R _L = 25 kΩ <u>4/</u>	1		95		
			2,3		60		
Slew rate	S _R	<u>5/</u>	4	All	15		V/ms
			5,6		7		
Gain-bandwidth	GBW		4	All	60		kHz
			5,6		45		

1/ Unless otherwise specified, V₊ = 3 V, 5 V or 15 V, V₋ = 0 V, V_{CM} = V_O = V₊/2, R_L > 1 MΩ.

2/ Limits are dictated by testing limitations and not device performance.

3/ Do not short circuit output to V₊ when V₊ is greater than 13 V as reliability will be adversely affected.

4/ V_{CM} = 7.5 V, R_L = connected to 7.5 V. For sourcing tests, 7.5 V ≤ V_O ≤ 11.5 V and for sinking tests, 3.5 V ≤ V_O ≤ 7.5 V.

5/ Device configured as a voltage follower, with a 10 V input step. For positive slew, V_{IN} swing is 2.5 V to 12.5 V, V_{OUT} is measured between 6.0 V and 9.0 V. For negative slew, V_{IN} swing is 12.5 V to 2.5 V, V_{OUT} is measured between 9.0 V and 6.0 V.

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Device types	01	02
Case outlines	P	C and X
Terminal number	Terminal symbol	
1	OUTPUT 1	OUTPUT 1
2	IN 1-	IN 1-
3	IN 1+	IN 1+
4	V-	V+
5	IN 2+	IN 2+
6	IN 2-	IN 2-
7	OUTPUT 2	OUTPUT 2
8	V+	OUTPUT 3
9	---	IN 3-
10	---	IN 3+
11	---	V-
12	---	IN 4+
13	---	IN 4-
14	---	OUTPUT 4

FIGURE 1. Terminal connections.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/	1,2,3,4,5,6 1/
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---

1/ PDA applies to subgroup 1.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-07-19

Approved sources of supply for SMD 5962-95603 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-9560301QPA	<u>3</u> /	LMC6462AMJ-QML
5962-9560302QCA	01295	LMC6464AMJ-QML
5962-9560302QXA	<u>3</u> /	LMC6464AMWG-QML

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE
number

01295

Vendor name
and address

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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